What is claimed is:

1. A method of forming a thin film transistor of a semiconductor integrated circuit, comprising:

forming a first conductive structure over a portion of the integrated circuit;

forming a first dielectric layer over the first conductive structure;

forming a polysilicon layer, having a first dopant therein, over the first dielectric layer;

forming a second dielectric layer over a portion of the polysilicon layer substantially over the first conductive structure;

doping, with a second dopant, the polysilicon layer not covered by the second dielectric layer;

forming a photoresist layer over a portion of the second dielectric layer and a portion of the polysilicon layer;

doping, with a third dopant, the polysilicon layer not covered by the second dielectric layer and the photoresist layer;

removing the photoresist layer;

forming oxide sidewall spacers adjacent to the second dielectric layer and covering a portion of the polysilicon layer adjacent to the second dielectric layer; and

doping, with the third dopant, the polysilicon layer not covered by the second dielectric layer and the sidewall spacers.

2. The method of claim 1, wherein the first conductive structure comprises a gate electrode of a field effect device.

3. The method of claim 1, wherein the first conductive structure has a thickness of between approximately 1000 to 2500 angstroms.

4. The method of claim 1, wherein the first dielectric layer comprises a gate oxide having a thickness of between approximately 200 to 400 angstroms.

5. The method of claim 1, wherein the first dielectric layer comprises an oxide/nitride composite having a thickness of between approximately 200 to 400

angstroms.

6. The method of claim 1, wherein the first dopant comprises an n-type dopant.

7. The method of claim 1, wherein the second dielectric layer comprises an oxide.

8. The method of claim 1, wherein the second dopant comprises a p^--type dopant.

9. The method of claim 1, wherein the polysilicon layer has a thickness of between approximately 300 to 800 angstroms.

10. The method of claim 1, wherein the third dopant comprises a p^+-type dopant.

11. A method of forming a thin film transistor of a semiconductor integrated circuit, comprising:

forming a polysilicon gate electrode over a portion of the integrated circuit;

forming a gate oxide layer over the gate electrode;

forming a conformal polysilicon layer over the gate oxide layer and a portion of the integrated circuit;

doping the polysilicon layer with an n-type dopant to form a channel region over the gate electrode;

forming a screen oxide layer over a portion of the polysilicon layer substantially over the gate electrode;

doping, with a p^--type dopant, the polysilicon layer not covered by the screen oxide layer to form a lightly doped drain region on each side of the channel region;

forming a photoresist layer over a portion of the screen oxide layer and one of the lightly doped drain regions;

doping, with a p^+-type dopant, the polysilicon layer not covered by the photoresist layer;

removing the photoresist layer;

forming a conformal oxide layer over the integrated circuit;

patterning and etching the conformal oxide layer to form sidewall spacers on the sides of the screen oxide layer and the polysilicon layer adjacent to the screen oxide layer;

doping, with a p^+-type dopant, the polysilicon layer not covered with the screen oxide layer or the sidewall oxide spacers; and

removing the screen oxide layer and the sidewall oxide spacers.

12. The method of claim 11, wherein the n-type dopant comprises phosphorous.

13. The method of claim 11, wherein the p^--type dopant comprises BF_2 wherein the polysilicon has a dopant concentration of between approximately 10^{12} to $10^{13}/cm^2$.

14. The method of claim 11, wherein the p^+-type dopant comprises BF_2 wherein the polysilicon has a dopant concentration of approximately $10^{15}/cm^2$.

15. A structure consisting of a portion of an integrated circuit, comprising:

a gate electrode;

a gate oxide layer disposed over the gate electrode;

an n-channel polysilicon region substantially centered over the gate electrode;

a p^+-type source region adjacent to a first end of the n-channel region;

a p-type lightly doped drain region adjacent to a second end of the n-channel region; and

a p^+-type drain region adjacent to the p-type lightly doped drain region.

16. The structure of claim 15, wherein the n-channel region comprises phosphorous.

17. The structure of claim 16, wherein the p-type lightly doped drain region comprises BF_2 having a dopant concentration of between approximately 10^{12} to $10^{13}/cm^2$.

18. The method of claim 15, wherein the p^+-type regions comprise BF_2 having a dopant concentration of approximately $10^{15}/cm^2$.

19. A method of forming a thin film transistor of a semiconductor integrated circuit, comprising:

forming a first conductive structure over a portion of the integrated circuit;

forming a first dielectric layer over the first conductive structure;

forming a polysilicon layer, having a first and a second end, over the first dielectric layer;

forming a channel region in the polysilicon layer substantially over the first conductive structure;

forming a source region in the polysilicon layer adjacent to the first end of the channel region;

forming a LDD region in the polysilicon layer adjacent to the second end of the channel region; and

forming a drain region in the polysilicon layer adjacent to the LDD region.